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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,247	09/24/2003	Perry Lea	200207569-1	3532

22879 7590 10/02/2008

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
CHENG, PETER L	
ART UNIT	PAPER NUMBER
2625	

NOTIFICATION DATE	DELIVERY MODE
10/02/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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JERRY.SHORMA@HP.COM
mkraft@hp.com
ipa.mail@hp.com

ADVISORY ACTION

Response to Arguments

1. The following is a copy of a response to arguments cited in the final action. Applicant's arguments filed 4/24/2008 have been fully considered but they are not fully persuasive.

Regarding claim 1, with respect to applicant's argument that

> *the "arrangement of elements and configuration of the dual bus is not taught or suggested by references";* **page 11, 4th paragraph.**
>
> *"A page frame buffer (being a separate element from the cache memory 403) is not present and not part of the G bus and B bus configuration. Thus, the claimed page frame buffer and the claimed arrangement with the recited dual bus system is not taught by the G and B buses of SHISHIZUKA";* **page 11, 5th paragraph.**

has been considered.

In reply,

> As noted in the claim rejection, SHISHIZUKA cites, "This controller consists of a FIFO which is a buffer to transfer image data to the printer by way of the GBI (G

bus/B bus I/F) and a circuit which controls the FIFO"; **col. 44, lines 14 – 18.** As shown in **Fig. 66,** the FIFO controller 6603 is a component of the "printer controller" **4303**; **col. 4, line 61.** As shown in **Fig. 4** and **Fig. 91,** the "printer controller" **4303** is a component of the "DoEngine".

SHISHIZUKA's "printer FIFO" (i.e., "page frame buffer") is contained in a printer image data transfer FIFO controller 6603 which, in turn, is *connected to the G and B buses by means of the GBI (G bus/B bus I/F) interface*.

Regarding claim 1, with respect to applicant's argument that

"Thus the first and second buses explained by the Office Action comprise multiple components connected by interface ports (e.g. I/F) and multiple communication paths, none of which teaches the dual bus that can transmit image data from the scanner to the memory simultaneously with transmitting the page of data from the page frame buffer to the imaging mechanism"; **page 12, 5th paragraph.**

and regarding the "scanner video I/F connections and components" shown in ***Fig. 45*** *of SHISHIZUKA and the "printer controller 4303 components and connections including the printer device I/F" shown in* ***Figs. 66 – 67*** *of SHISHIZUKA, the multiple channels and paths relied upon by the examiner*

cannot constitute a first or second bus, and fail to teach or suggest a first bus and a second bus as proposed by the Office Action"; **page 12, 5th paragraph.**

has been considered.

In reply,

SHISHIZUKA teaches a first bus (i.e., from the interface "VIDEO I/F TO SCANNER" to the "Scanner Controller" **4302** to either of the G bus or B bus (by means of a "G Bus/B Bus I/F" **4301A**) which is connected to SDRAM by means of a "System Bus Bridge" **402,** "MC Bus", "SDRAM & ROM Controller (MC)" **403,** and "Memory BUS", all shown in **Fig. 4**) which connects the "scanner to the memory" and a second bus (i.e., from the "Printer Controller" **4303** containing the printer controller FIFO to the printer and is shown as "VIDEO I/F TO PRINTER" in **Fig. 4**) which connects the "page frame buffer to the imaging mechanism". Data can be transmitted from the scanner to memory while simultaneously transmitting data from the page frame buffer to the printer.

SHISHIZUKA teaches that the DoEngine's "dual-bus configuration can solve the problem on occupation of the bus, and allows accessing the CPU and memory in parallel. Data can be output in parallel with input of data"; **col. 73, lines 31 – 34.**

With this configuration and with reference to **Fig. 113B**, SHISHIZUKA teaches that by using the DoEngine, a case "where processing is done *in parallel* in units of pages using a scanner and printer as device examples"; **col. 73, lines 44 – 46** and **col. 73, line 60 – col. 74, line 10.** SHISHIZUKA further cites, "This configuration is different from the prior art in that input data and output data can be processed in parallel and the trap of data is cancelled"; **col. 74, lines 13 – 15.**

It should be noted that SHISHIZUKA provides detail at a lower "functional block level", whereas, applicant's **Figs. 1** and **2** are higher "system level diagrams". Therefore, care should be taken when comparing the two inventions.

For example, even though SHISHIZUKA's first and second buses comprise "multiple components", the applicant also has indicated that "*it will be appreciated that any number and configuration of data busses may be used to accommodate desired functions or preference. The operation and directional flow of the image data will be further explained with reference to Figure 2*"; **page 8, lines 6 – 8.**

This appears to be an admission that the actual implementation of the higher-level "system diagrams" may require additional components.

For example, applicant's "second bus" **185** shown in **Fig. 1** is illustrated as being composed of *one section* between the "page frame memory" **170** and an

"imaging processor" **180** (which converts the data page from the page frame memory **170** to a "print ready engine format"; **page 7, lines 1 - 3**), and *another section* between the "imaging processor" **180** and "imaging mechanism" **130.**

Access to a memory is typically made by use of a "memory bus" consisting of address, data and control lines, whereas, *communications* with an "imaging mechanism" is typically made by a bus consisting of data and control lines. This suggests that the two sections of the "second bus" may not be the same.

Similarly, applicant's "first bus" **155** shown in **Fig. 1** is illustrated as being composed of *one section* between the "scanner" **110** and the "controller" **140**, and *another section* between the "controller" **140** and the "main memory" **150**. As noted, access to a memory is typically made by use of a "memory bus" consisting of address, data and control lines, however, applicant also suggests that "data pages can then be sent and loaded into a formatter 120 by, for example, a FIREWIRE® bus or other type of bus using another desired communication protocol"; **page 4, lines 25 – 27.**

Regarding claim 1, with respect to applicant's argument that

the statement cited in the previous action on ***page 6, last paragraph****, "'data can be transmitted from the scanner to memory while simultaneously transmitting data from the page frame buffer to the printer' is not supported by SHISHIZUKA*

and no citation to an actual teaching in SHISHIZUKA is provided. Accordingly, SHISHIZUKA fails to teach or suggest the elements relied upon by the rejection"; **page 13, 1st paragraph.**

has been considered.

In reply,

As noted above, SHISHIZUKA teaches that the DoEngine's "dual-bus configuration can solve the problem on occupation of the bus, and allows accessing the CPU and memory in parallel. Data can be output in parallel with input of data"; **col. 73, lines 31 – 34.**

Specifically, with reference to **Fig. 113B**, SHISHIZUKA teaches that by using the DoEngine, a case "where processing is done *in parallel* in units of pages using a scanner and printer as device examples"; **col. 73, lines 44 – 46** and **col. 73, line 60 – col. 74, line 10.** SHISHIZUKA further cites, "This configuration is different from the prior art in that input data and output data can be processed in parallel and the trap of data is cancelled"; **col. 74, lines 13 – 15.**

Regarding claim 1, with respect to applicant's argument that

"WESTERVELT fails to teach or suggest how its FIFO buffer would be connected and where it would be connected into the DoEngine of SHISHIZUKA. Indeed the

DoEngine already includes a cache memory 403 (figure 4) and the printer controller 4303 already includes a FIFO buffer 6608 (figure 66)"; **page 13, 2nd paragraph.**

"Thus, the motivation to combine provided by the Office Action (page 7, 3rd paragraph) is not supported by the references. Rather, the combination is made using impermissible hindsight using the claims as a blueprint. The rejection is improper"; **page 13, 2nd paragraph.**

has been considered.

In reply,

SHISHIZUKA teaches a "page frame buffer" which operates with the "G bus and B bus configuration". As shown in **Fig. 77**, SHISHIZUKA teaches buffering the "page memory" data in a "printer FIFO" which is contained in a printer image data transfer FIFO controller 6603. "This controller consists of a FIFO which is a buffer to transfer image data to the printer by way of the GBI (G bus/B bus I/F) and a circuit which controls the FIFO"; **col. 44, lines 14 – 18.** As shown in **Fig. 66,** the FIFO controller 6603 is a component of the "printer controller" **4303**; **col. 4, line 61.** As shown in **Fig. 4** and **Fig. 91,** the "printer controller" **4303** is a component of the "DoEngine".

WESTERVELT teaches a "page frame buffer" which can be configured to store "a scanline, band, page or plane" of data; **page 6, paragraph 124, lines1 – 4.**

Since SHISHIZUKA does not specifically teach a page frame buffer (i.e., the "printer FIFO") as being configured to store *a page of data*, the WESTERVELT reference teaches that the size of the "printer FIFO" can be made to accommodate not only pages of data but also scanlines, bands or planes of data. That is, it would have been obvious to one of ordinary skill in the art at the time the invention was made to match the size of the "printer FIFO" with the "imaging mechanism". For example, laser printers require page-sized memories, whereas, a scanning inkjet printer would require a smaller band-sized memory.

Regarding claim 1, with respect to applicant's argument that

the previous office action's citation of SHISHIZUKA's timing signals VSYNC and HSYNC signals on ***pages 5 - 6*** *fails to "teach or suggest simultaneous or parallel transmission of data by a dual bus transferring data from page memory to the imaging mechanism while also transferring image data from a scanner to main memory";* **page 14, 1st paragraph.**

has been considered.

In reply,

SHISHIZUKA teaches that "the image data is output in synchronization with these signals. The scanner controller (SCC) acquires the image data in synchronization with the timing signals" VSYNC and HSYNC; **col. 66, lines 43 – 46.**

As noted above, SHISHIZUKA teaches that the DoEngine's "dual-bus configuration can solve the problem on occupation of the bus, and allows accessing the CPU and memory in parallel. Data can be output in parallel with input of data"; **col. 73, lines 31 – 34.**

Specifically, with reference to **Fig. 113B**, SHISHIZUKA teaches that by using the DoEngine, a case "where processing is done *in parallel* in units of pages using a scanner and printer as device examples"; **col. 73, lines 44 – 46** and **col. 73, line 60 – col. 74, line 10.** SHISHIZUKA further cites, "This configuration is different from the prior art in that input data and output data can be processed in parallel and the trap of data is cancelled"; **col. 74, lines 13 – 15.**

Regarding claim 2, with respect to applicant's argument that

"no such first or second bus is taught or suggested."; **page 14, 2nd paragraph.**

has been considered with respect to **claim 1**.

Regarding claim 11, with respect to applicant's argument that

> *the previous office action's citation of SHISHIZUKA's timing signals VSYNC and HSYNC signals on* ***page 12*** *"are not image data pages that are generated from scanning sheets of print media as recited in the claim, and the timing signals are not image data pages loaded into a memory";* **page 15, 2nd paragraph.**
>
> *"As such, the VSYNC and HSYNC timing signals, as well as the processing of the timing signals, are irrelevant to the claimed elements. Thus, the cited text fails to teach or suggest 'transmitting the first image data page for imaging to an imaging mechanism where the transmitting occurs in parallel with the loading' as recited in claim 11";* **page 15, 3rd paragraph.**

has been considered.

In reply,

> As noted for claim 1, SHISHIZUKA teaches that "the image data is output in synchronization with these signals. The scanner controller (SCC) acquires the image data in synchronization with the timing signals" VSYNC and HSYNC; **col. 66, lines 43 – 46.**
>
> As previously noted, SHISHIZUKA teaches that the DoEngine's "dual-bus configuration can solve the problem on occupation of the bus, and allows

accessing the CPU and memory in parallel. Data can be output in parallel with input of data"; **col. 73, lines 31 – 34.**

Specifically, with reference to **Fig. 113B**, SHISHIZUKA teaches that by using the DoEngine, a case "where processing is done *in parallel* in units of pages using a scanner and printer as device examples"; **col. 73, lines 44 – 46** and **col. 73, line 60 – col. 74, line 10.** SHISHIZUKA further cites, "This configuration is different from the prior art in that input data and output data can be processed in parallel and the trap of data is cancelled"; **col. 74, lines 13 – 15.**

Regarding claim 17, with respect to applicant's argument that

"SHISHIZUKA fails to teach or suggest the recited arrangement of a first data bus, a second data bus, and parallel transmission of data between components as recited in claim 17"; **page 16, 1st paragraph.**

With regards to WESTERVELT's teaching a FIFO buffer, "as explained under claim 1, the combined references still fail to establish a prima facie obviousness rejection"; **page 15, 2nd paragraph.**

has been considered with respect to **claims 1** and **2**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peter L. Cheng whose telephone number is 571-270-3007. The examiner can normally be reached on MONDAY - FRIDAY, 8:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, King Y. Poon can be reached on 571-272-7440. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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September 26, 2008